Design And Validation Of XOR XNOR Hybrid Full Adder Utilizing 32 Nm Technology

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ABSTRACT

This study use 32nm FinFET technology to develop and analyze a CMOS full adder, aiming to overcome the limitations of traditional bulk CMOS at deep submicron nodes. FinFETs have been the best choice for low-power, high-performance digital circuits because they better regulate short-channel effects and have fewer leakage currents. We use FinFETs in both static and dynamic logic styles to design the entire adder, which is a core part of arithmetic and logic circuits. We then test its performance measures, such as power consumption, latency, and power-delay product (PDP). The proposed architecture leverages the benefits of FinFETs' double-gate topology to achieve an optimal balance between speed and power efficiency. We used industry-standard tools to do comparative simulations to see how well the FinFET-based complete adder worked compared to its bulk CMOS counterpart. The results demonstrate big improvements in energy economy, switching speed, and overall scalability. This means that the design is good for future high-speed, low-power integrated circuits.Keywords : ALU, Low power consumption, low delay,

I.INTRODUCTION

A key goal in designing digital circuits is to make full adders that are both fast and use less power. This is especially important because there is an increasing need for high-performance computing in areas like signal processing, image processing, and AI. Researchers have examined numerous circuit topologies and logical methodologies to achieve these objectives. One such method is to utilize a high-performance 10-transistor (10T) XOR-XNOR cell in a hybrid-logic full adder. The main job of full adders is Full adders are the basic parts of arithmetic logic units (ALUs), which processors need to do math. The speed and power utilization of a digital system depend directly on how well a full adder works [2]. Some traditional CMOS full adder designs have problems with speed, power use, or space efficiency. Because of this, modern digital systems need unique circuit designs to meet their strict requirements. This design method uses the best parts of numerous logic architectures, such as pass-transistor, transmission gate, and CMOS logic. By properly mixing several logic

models, it is possible to make the whole adder faster, use less power, and take up less space. This plan needs a special 10-transistor cell that can make both XOR and XNOR outputs at the same time. This simultaneous generation saves area and propagation latency by getting rid of the need for separate XOR and XNOR gates. The design of the 10T cell includes low power use and maximum driving strength [3]. Section I of this work serves as an introduction. Part II is an overview of the literature. Part III: The current method. Section IV talks about the proposed method, and Section V talks about the conclusion and what could happen in the future.

II. LITERATURE SURVEY

A literature review of high-speed hybrid-logic full adders using high-performance 10-T XOR-XNOR cells shows that a lot of work has gone into improving important performance measures like speed, power use, and space efficiency [4]. Here is a summary of the main findings and trends. Cell Optimization for XOR-XNOR is A lot of research goes into making effective XOR-XNOR cells because they are necessary for making complete adders. The 10-T architecture is widely studied because it can make XOR and XNOR outputs at the same time, which speeds up propagation delay. Researchers are continually attempting to make these cells more powerful and able to swing more. Hybrid-Logic Methods are [5] To gain the optimum performance, it is common to use more than one type of logic, such as CMOS, transmission gate logic, and pass-transistor logic. By taking advantage of the best parts of each logic style, hybrid designs make full adders that are faster, use less power, and take up less space [6]. There are metrics for performance that are The power-delay product (PDP) is a common way to measure how well full adder circuits work as a whole. Researchers want to lower PDP by reducing down on both power use and propagation latency.

III. EXISTING METHOD

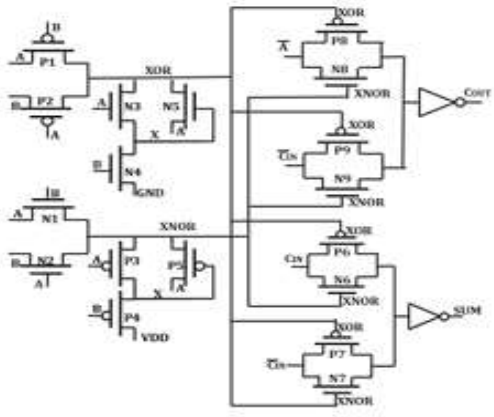

Fig.1.26 Transistor based Full adder

Twenty-six transistors are also used to make this structure. The CMOS logic style is used to implement modules II and III of the FA cell's design-1 (FA4), as seen in Fig.1. This circuit is the best at what it does, which is PDP throughout every FA cell. Using 26 transistors, this FA makes the sum and carry (COUT). [7] The architecture in Fig. 1 is employed to make Module II of this FA cell. Module I sends out XOR and XNOR signals that this circuit utilizes to control a pMOS and a nMOS (P8 and N8). The source and drain terminals of transistors P8 and N8 are connected to each other through the output node (SUM) and CIN, respectively. The output is connected to CIN, and XOR and XNOR are at logic "0" and "1," respectively, when transistors P8 and N8 are "ON." But when XOR and XNOR [8] are at logic "1" and logic "0," respectively, the output is connected to ground by N6 and N7. In this case, logic "0" at CIN will connect the complete output to VDD through P6 and P7. The design in Fig. 1 is used to make Module III of this FA cell. This circuit sends CIN through TG to set the XOR input to logic "1." When XNOR is at logic "1," both transistors output A. Instead, it sends A and B from different TG transistors to the inputs.

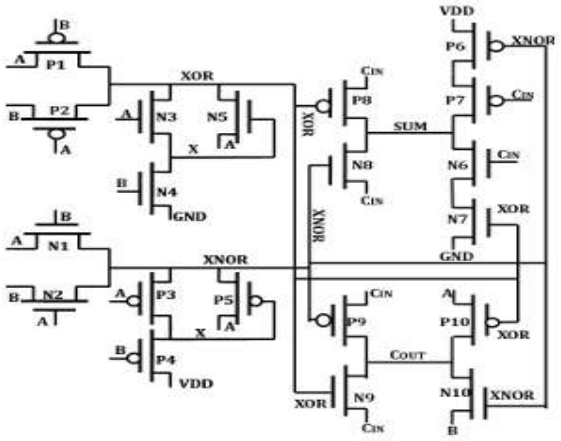

Fig .2.20 Transistor based Full adder

This FA employs 20 transistors to make the sum and carry (COUT). In Fig. 2, you can see that the FA cell design-4 (FA4) uses the CMOS [9] logic style to build modules II and III. This circuit is the best for PDP when it comes to performance across all FA cells. This FA employs 20 transistors to add and carry (COUT). The design for Module II of this FA cell is based on Figure 4. This circuit uses XOR and XNOR signals from Module I to open and close a pMOS and a nMOS (P8 and N8). The output node (SUM) and CIN connect the source and drain terminals of both transistors P8 and N8. The output is connected to CIN, and transistors P8 and N8 are in the "O[10] N" state. XOR and XNOR are at logic "0" and "1," respectively. But when XOR is at logic "1" and XNOR is at logic "0," the output is connected to ground by N6 and N7 for high logic at CIN. In this

situation, P6 and P7 will connect the complete output to VDD via logic "0" at CIN. Figure 2 shows how to make this FA cell's Module III. This circuit sets the XOR input to logic "1" by sending CIN through TG. When XNOR is at logic "1," it sends A and B from different TG transistors instead of sending A from both transistors. This spreads the load across the inputs.

IV.PROPOSED METHOD

A. Fin-FET Full adder using 26 Transistor

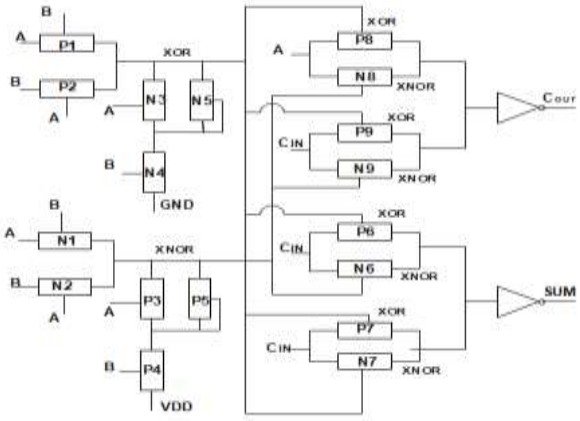

Fig 3. Proposed design 3 using 26 transistor using 32 nm finfet technology

In the below diagram, the p1 transistor back gate is connected to front gate of same transistor and similarly for N1 transistor the front gate and back gate are connected together with Cin as input .In p1 the drain terminal is connected to the drain terminal of N1 transistor. And the source terminal of the p1 transistor is connected to VDD [11]and the source terminal of N1 transistor is connected to ground, from the drain terminal of both the transistors we take output as CinBar1. In the below diagram, the p2 transistor back gate is connected to front gate of same transistor and similarly for N2 transistor the front gate and back gate are connected together with ABar1 as input .In p2 the drain terminal is connected to the drain terminal [12] of N2 transistor. And the source terminal of the p2 transistor is connected to VDD and the source terminal of N2 transistor is connected to ground .from the drain terminal of both the transistors we take output as ABar2.

In the below diagram, the p3 transistor back gate is connected to front gate of same transistor and similarly for N3 transistor the front gate and back gate are connected together with CinBar as input .In p3 the drain terminal is connected to the drain terminal of N3 transistor. And the source terminal of the p3 transistor is connected to VDD and the source terminal of N3 transistor is connected to ground .from the drain terminal of both the transistors we take output as CinBar2.

In p4 transistor front gate is connected to back gate through input B and the drain is connected to input A .and the source is connected to drain of p5 transistor .in p5 transistor the front gate is connected to back gate through input A .The source is connected to input B .source of p4 is connected to drain of N4 .front gate is connected to back gate of N4 transistor. The N4 transistor source is connected to drain of N5 transistor.in N5 the front gate is connected to back gate through input B .and source of N5 is grounded . The drain of N5 is connected to source of N4 and front gate of N6 .and In N6 the back gate is connected to front gate .to the drain terminal input is given as A .The N5 transistor input is connected to source terminal of N6 and performs XOR operation.

In N7 transistor the front gate is connected to back gate of the transistor with input B and source terminal is connected the input A .and the N8 transistor back gate is connected to front gate with the input A. And the drain terminal is connected to input B and the drain terminal of N7 and source terminal of N8 is connected together. In transistor p6 the back gate is connected to front gate through input A and similarly in p7 the back gate is connected to front gate through input B in p7 the drain is connected to VDD P6 drain is connected to source of p7 and connected to front gate of p8 and the front gate of p8 is connected to back gate of p8 ,the source terminal of p8 transistor given through input A. The P6 source terminal and p8 drain terminal are connected together to perform XNOR operation .The p9 transistor back gate is connected to front gate of same transistor and similarly for N9 transistor the front gate and back gate are connected together with A as input .In p9 the drain terminal is connected to the drain terminal of N9 transistor. And the source terminal of the p9 transistor is connected to VDD and the source terminal of N2 transistor is connected to ground .from the drain terminal of both the transistors we take output as ABar1.

The drain of p10 and drain of N10 are connected with the input ABar2. the p10 transistor front gate is connected to back gate and similarly in the N10 transistor the front gate is connected to back gate and performs XOR operation .source of p10 and N10 are connected together and given as output Cout. The p11 front gate and back gate are connected together and N11 front gate and back gate are connected together. Drain of p11 and N11 and given through input CinBar2 ,source of P11 and N11 are connected and taken output as Cout .SThe N12 front gate and back gate are connected and given to front gate of N11 transistor .Drain of N12 is connected to drain of p12 with input CinBar .Source of N12 connected with source of p12 and given as output sum .P12 front gate is connected to back gate .In p13 transistors front gate and back gate are connected together and performs XNOR gate, Drain is connected to N13 with input CinBar2.front gate and back gate are connected and performs XOR operation source of p13 is connected to source of N13 sand taken output as sum.

B.Fin-FET Full adder using 20 Transistor

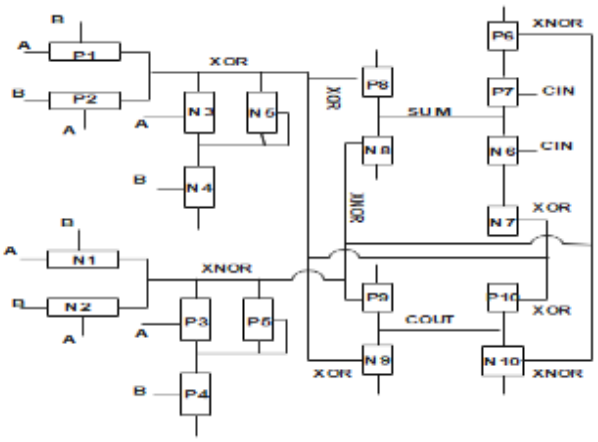

Fig 4. Proposed design 4 using 20 transistor using 32 nm finfet technology

The circuit below is a 4-bit binary Full Adder made up of transistors. The circuit is made up of both PMOS and NMOS transistors. The back gate [13] of the transistor P1 is usually linked to B and the front gate of P1. A is connected to the drain of P1. The source of P1 is linked to the drain of P2 and the front and rear gates of the N3 transistor. The front and back gates of N5 are connected to the source of N3, while the drain of N4 is connected to the source of N3. A is connected to the drain of N5. The XOR branch is linked to the source of N5. B connects to the front and back gates of N4. VDD is associated to the source of N4. A is connected to the drain of P2. The back gate of P2 leads to the front gate of P2. The front gate of N1 is usually connected to B and the back gate of N1. [14] The drain of N1 is linked to the source of N2, the source of P3, and the drain of P5. N2's drain is linked to A. N2's front and back gates are Connected B. A is connected to the front and back gates of P3. The drain from P3 goes to the front and back gates of P5. A is where P5 comes from. The drain of P4 goes to both B and VDD. The entrance and back gates of P4 are linked to each other. The XOR branch connects the front and back gates of P6. Cin is related to the source of P6. The P6 drain and the N6 drain are linked. The front and rear gates of N6 are connected to the front and back gates of P7. Cin is linked to the source of N6. Cin is related to the source of P7. The P7 drain is linked to the N7 drain. Cin is associated to the source of N7. The XOR branch connects the back and front gates of N7. VDD is connected to the drain of the P8 transistor. The front and rear gates of transistor P8 are linked together. The drain of P9 is connected to the source of P8. Cin is connected to all of P9's gates. The source of N8 is linked to the source of P9. Cin connects the front and back gates of N8. The drain of N8 is connected to the source of N9. The front and back gates of N9 are linked. The N9 drain is grounded. A is connected to the drain of P10. The branch of XOR connects the back and front gates of P10. The source of P10 is linked to the source of N10. The XNOR branch connects the back and front gates of Transistor N10. The drain of Transistor N10 is linked

to A. The common point of the drain for P7 and N7 is connected to the common point of the drain for P10 and N10. Cout is used as the source.

COMPARISON TABLE

Method	Static Power	Dynamic Power	Average Power
Design-1(μwatt)	29.7	64.58	52.7
FinFET-1 (pico-Watt)	4.82	0.67	1.5
Design2 μWatt	25.8	60.2	45.2
FinFET-2 (Nano-Watt)	18.2	18.56	17.3

V.CONCLUSION AND FUTURE SCOPE

We started by looking at the XOR/XNOR and XOR–XNOR circuits in this study. The evaluation showed that employing NOT gates on a circuit's critical path is a bad idea. One more bad thing about a circuit is that it has a positive feedback on the outputs of the XOR–XNOR gate to make up for the output voltage level. This feedback makes the circuit take longer to respond, use more power, and have more output capacitance. This paper describes the design and implementation of a high-speed hybrid-logic full adder that uses 32nm FinFET technology and a 10-transistor XOR–XNOR cell. The proposed design makes good use of the benefits of FinFET transistors, such as less short-channel effects, less leakage current, and faster switching speed. Low-power design is also becoming a big problem for high-performance digital systems like microprocessors, digital signal processors (DSPs), and other uses. The construction of exceedingly complex semiconductors with high clock frequencies is made possible by higher operating speeds and more chips per square inch. Low power design is also necessary to lower the power in high-end systems with a lot of integration density, which speeds up the operation.

REFERENCES

[1] N. S. Kim et al., “Leakage current: Moore’s law meets static power,” Computer, vol. 36, no. 12, pp. 68–75, Dec. 2003.

[2] N. H. E. Weste and D. M. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed. Boston, MA, USA: Addison-Wesley, 2010.

[3] S. Goel, A. Kumar, and M. Bayoumi, "Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 12, pp. 1309–1321, Dec. 2006.

[4] H. T. Bui, Y. Wang, and Y. Jiang, "Design and analysis of low-power 10-transistor full adders using novel XOR-XNOR gates," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 49, no. 1, pp. 25–30, Jan. 2002.

[5] S. Timarchi and K. Navi, "Arithmetic circuits of redundant SUT-RNS," IEEE Trans. Instrum. Meas., vol. 58, no. 9, pp. 2959–2968, Sep. 2009.

[6] J. M. Rabaey, A. P. Chandrakasan, and B. Nikolic, Digital Integrated Circuits, vol. 2. Englewood Cliffs, NJ, USA: Prentice-Hall, 2002.

[7] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," IEE Proc.-Circuits, Devices Syst., vol. 148, no. 1, pp. 19–24, Feb. 2001.

[8] K. Yano, A. Shimizu, T. Nishida, M. Saito, and K. Shimohigashi, "A 3.8-ns CMOS 16×16-b multiplier using complementary pass-transistor logic," IEEE J. Solid-State Circuits, vol. 25, no. 2, pp. 388–395, Apr. 1990.

[9] A. M. Shams, T. K. Darwish, and M. A. Bayoumi, "Performance analysis of low-power 1-bit CMOS full adder cells," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 10, no. 1, pp. 20–29, Feb. 2002. [10] N. Zhuang and H. Wu, "A new design of the CMOS full adder," IEEE J. Solid-State Circuits, vol. 27, no. 5, pp. 840–844, May 1992.

[11] N. Weste and K. Eshraghian, Principles of CMOS VLSI Design. New York, NY, USA: Addison-Wesley, 1985.

[12] P. Bhattacharyya, B. Kundu, S. Ghosh, V. Kumar, and A. Dandapat, "Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 10, pp. 2001–2008, Oct. 2015.

[13] M. Vesterbacka, "A 14-transistor CMOS full adder with full voltageswing nodes," in Proc. IEEE Workshop Signal Process. Syst. (SiPS), Oct. 1999, pp. 713–722.

[14] M. Alioto, G. Di Cataldo, and G. Palumbo, "Mixed full adder topologies for high-performance low-power arithmetic circuits," Microelectron. J., vol. 38, no. 1, pp. 130–139, 2007

[15] A. M. Shams and M. A. Bayoumi, "A novel high-performance CMOS 1-bit full-adder cell," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 47, no. 5, pp. 478–481, May 2000.

[16] M. Aguirre-Hernandez and M. Linares-Aranda, "CMOS full-adders for energy-efficient arithmetic applications," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 4, pp. 718–721, Apr. 2011.